ABSTRACT

A CAN microcontroller that supports a plurality of message objects, including a processor core that runs CAN applications, and a CAN/CAL module that processes incoming messages, and a data memory. The data memory includes a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects. The memory-mapped registers for each message object contain respective command/control fields for configuration and setup of that message object. The CAN microcontroller further includes a memory interface unit that permits the processor core and the CAN/CAL module to concurrently access a different respective one of the first and second memory segments, and that arbitrates access to the same one of the first and second memory segments when the processor core and the CAN/CAL module request concurrent access to the same one of the first and second memory segments. In a second embodiment, the data memory includes a first memory space that is located on an integrated circuit chip on which the CAN microcontroller and the CAN/CAL module are incorporated, and a second memory space that is located off the integrated circuit chip. The first memory space includes a first memory segment that provides at least a portion of a message buffer memory space, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects. With this second embodiment, the CAN microcontroller further includes a memory interface unit that permits the processor core and the CAN/CAL module to concurrently access a different respective one of the first and second memory spaces, that permits the processor core and the CAN/CAL module to concurrently access a different respective one of the first and second memory segments, and that arbitrates access to the second memory space and that arbitrates access to the same one of the first and second memory segments when the processor core and the CAN/CAL module request concurrent access to the second memory space or to the same one of the first and second memory segments.